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(54) Transition metal clad interconnect for integrated circuits.

(57) An integrated circuit includes a patterned aluminum based interconnect clad on the top (15) and side portions (18,20) with a layer of transition metal (16,22). The cladding of transition metal prevents the formation of both vertical hillocks and lateral protrusions. Preventing these formations increases the reliability of an interconnect by significantly reducing passivation cracking and electrical shorting between interconnects which result from vertical hillock and lateral protrusion formations.

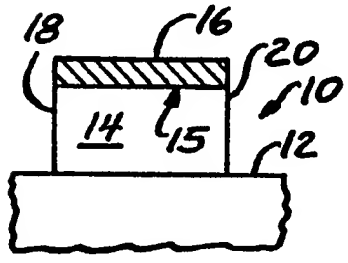

FIG. 1(a)

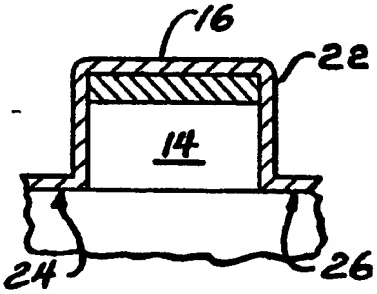

FIG. 1(b)

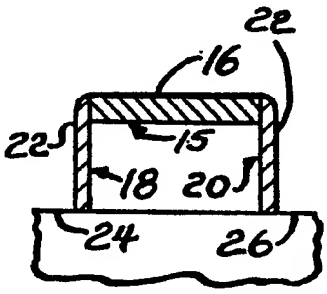

FIG. 1(c)

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Wafer 54 includes a silicon substrate 56 with circuit elements formed therein represented illustratively by an N+ region 58. Additionally, wafer 54 includes a dielectric film 60 and a polycrystalline silicon film 62 which are grown or deposited on silicon substrate 56 and patterned into various structures as dictated by the process and circuit design. Photolithography and etching techniques are used to form contact openings 64 to expose circuit elements formed in and on substrate 56.

As shown in FIG. 4(b), an interconnect member is then formed joining circuit element 58 to polycrystalline silicon 62. While any of the embodiments illustrated in FIGS. 1-3 could be used, the preferred embodiment is that of interconnected member 50 illustrated in FIG. 3(a). Interconnect member 50 is spaced from semiconductor substrate 56 and from the circuit elements formed therein and thereon by dielectric 60, except at selected contact openings 64 formed to expose those elements that are to be interconnected. In the embodiment shown, diffusion barrier 52 is first formed in order to prevent metallurgic reaction between the exposed silicon and subsequently formed metal layers. While diffusion barrier 52 has been illustrated as a layer formed over dielectric 60, it is to be understood that diffusion barrier 52 could be selectively deposited by chemical vapor deposition to fill only contract openings 64, and not to cover dielectric layer 60. Aluminum-silicon alloy 14 is then formed followed by the formation of transition metal layer 16, as described above.

Layers 52, 14 and 16 are then patterned in the same photolithographic etch process. Processing of interconnect member 50 then proceeds in the manner described above in reference to FIGS. 3-(b) and 3(c) to produce an interconnect according to the present invention having a transistor metal cladding on top and sides.

The interconnect according to the present invention will find wide applications in integrated circuits of varying sorts. It can be used in memories, processors, and other integrated circuits. Illustratively, within a semiconductor memory, there are numerous circuits such as row address buffers, clock generators, sense amplifiers, data lines, input and output buffers and various decoders. These circuits are interconnected by conductors, frequently metal. An interconnect, according to the present invention, can be used for such connections. Numerous uses will become apparent to the art.

The invention is not limited to the details of the foregoing examples. For example, the sequence in which some of the steps are practiced may be altered to suit a particular application or processing environment.

Claims

1. An interconnect for an integrated circuit having a substrate, comprising an interconnect member (10) formed of an aluminum-based metal established on the substrate and patterned into a desired interconnection pattern having a top surface (15) and side surfaces (18,20); and a conformal layer (22) of a transition metal established over the patterned interconnect member (10) to cover the top (15) and sides (18,20) of the patterned interconnect member (10) such that the transition metal covering prevents the formation of vertical hillocks and lateral protrusions.

2. An interconnect as claimed in Claim 1 wherein said interconnect member (10) comprises a homogeneous alloy of aluminum-silicon in which the silicon concentration is between 0.5 to 2.0 weight percent.

3. An interconnect as claimed in Claim 1 wherein said interconnect member comprises a homogeneous alloy of aluminum-silicon-titanium in which the silicon concentration is between 0.5 to 2.0 weight percent and the titanium concentration is between 0.1 and 0.5 weight percent.

4. An interconnect as claimed in Claim 1 wherein said interconnect member comprises a composite structure of alternating layers of titanium and layers of aluminum alloys.

5. An interconnect as claimed in any preceding claim further comprising a base located beneath said interconnect member (10), said base comprising a diffusion barrier layer that is patterned together with said interconnect member (10).

6. An interconnect as claimed in Claim 5 wherein said diffusion barrier is titanium nitride.

7. An interconnect as claimed in any preceding claim wherein said transition metal on said top surface (15) is the same as said transition metal on said side surfaces (18,20) of said interconnect member (10).

8. An interconnect as claimed in Claim 7 wherein said transition metal on said top surface (15) and said side surfaces (18,20) is titanium.

9. An interconnect as claimed in Claim 1 wherein said transition metal on said top surface (15) is different from said transition metal on said side surfaces (18,20) of said interconnect member (10).

10. An interconnect as claimed in Claim 9 wherein said transition metal on said top surface (15) is titanium and said transition metal on said side surfaces (18,20) of said interconnect member (10) is tungsten.

11. A method of forming an interconnect for an integrated circuit comprising forming an interconnect film (14) on an integrated circuit surface (12); forming a transition metal layer (16) on top of the